*Fig. 1B*

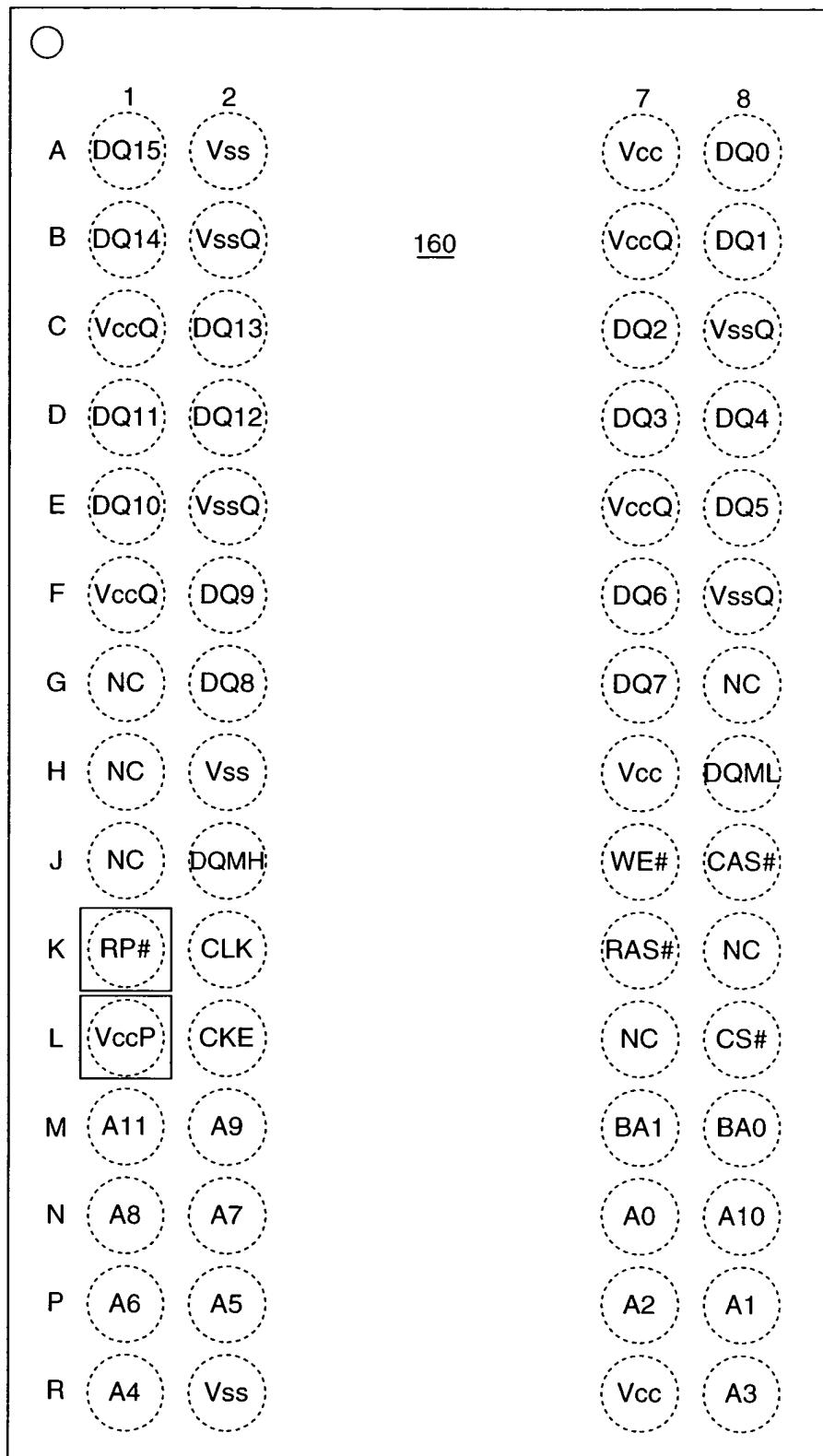
*Fig: 1C*

Fig. 2A

Fig. 2B

Fig. 2

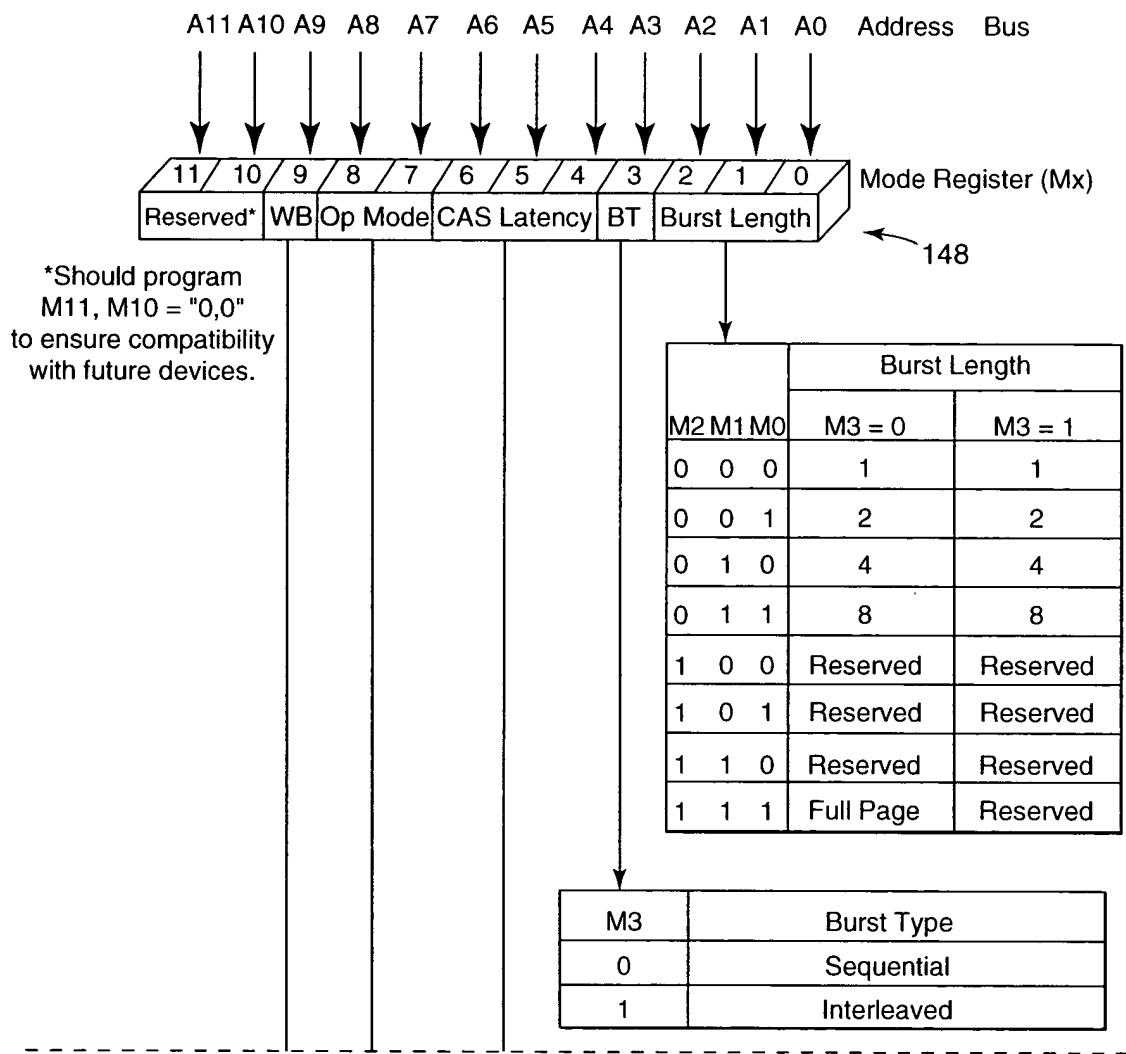
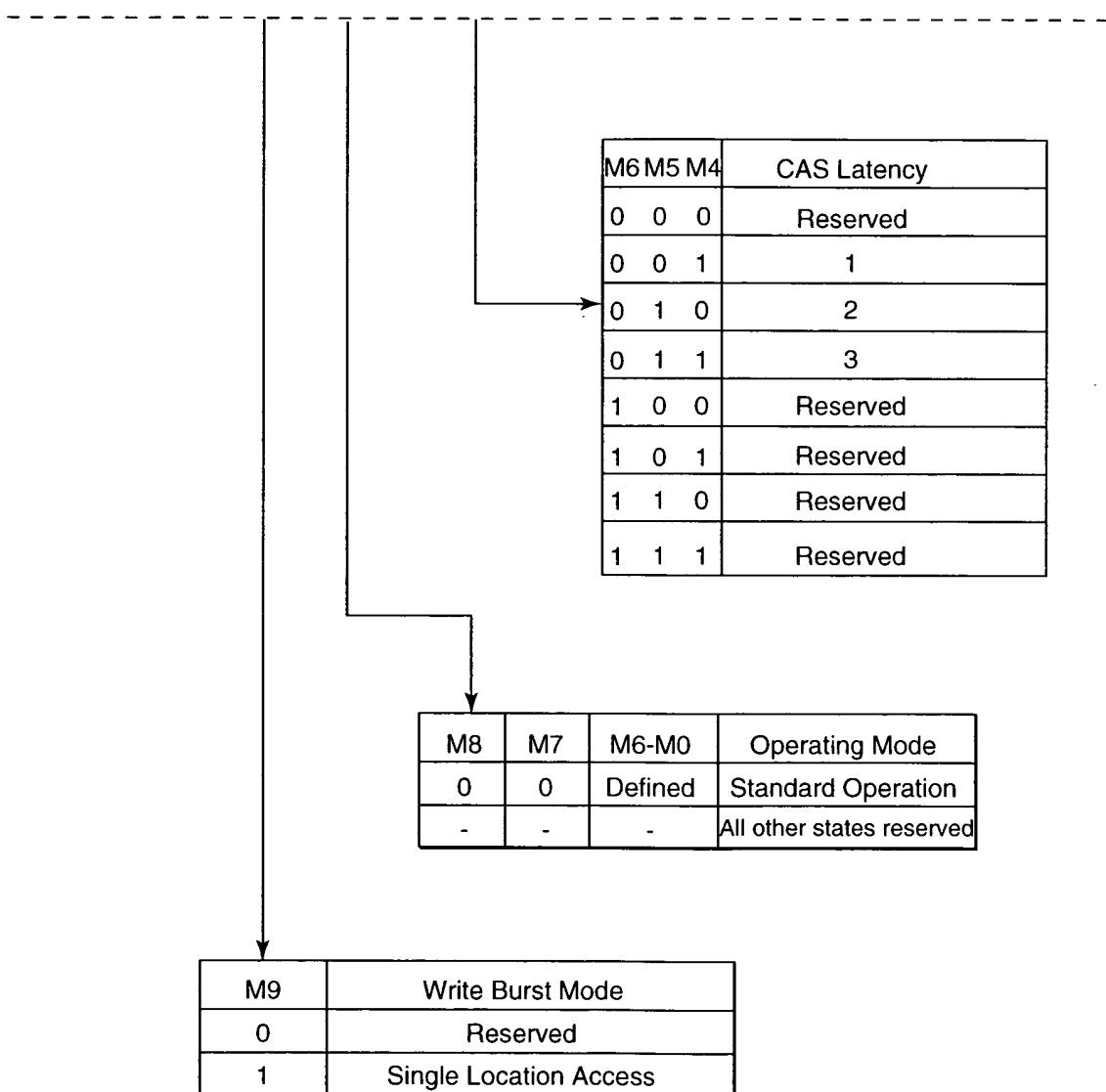


Fig. 2A

*Fig. 2B*

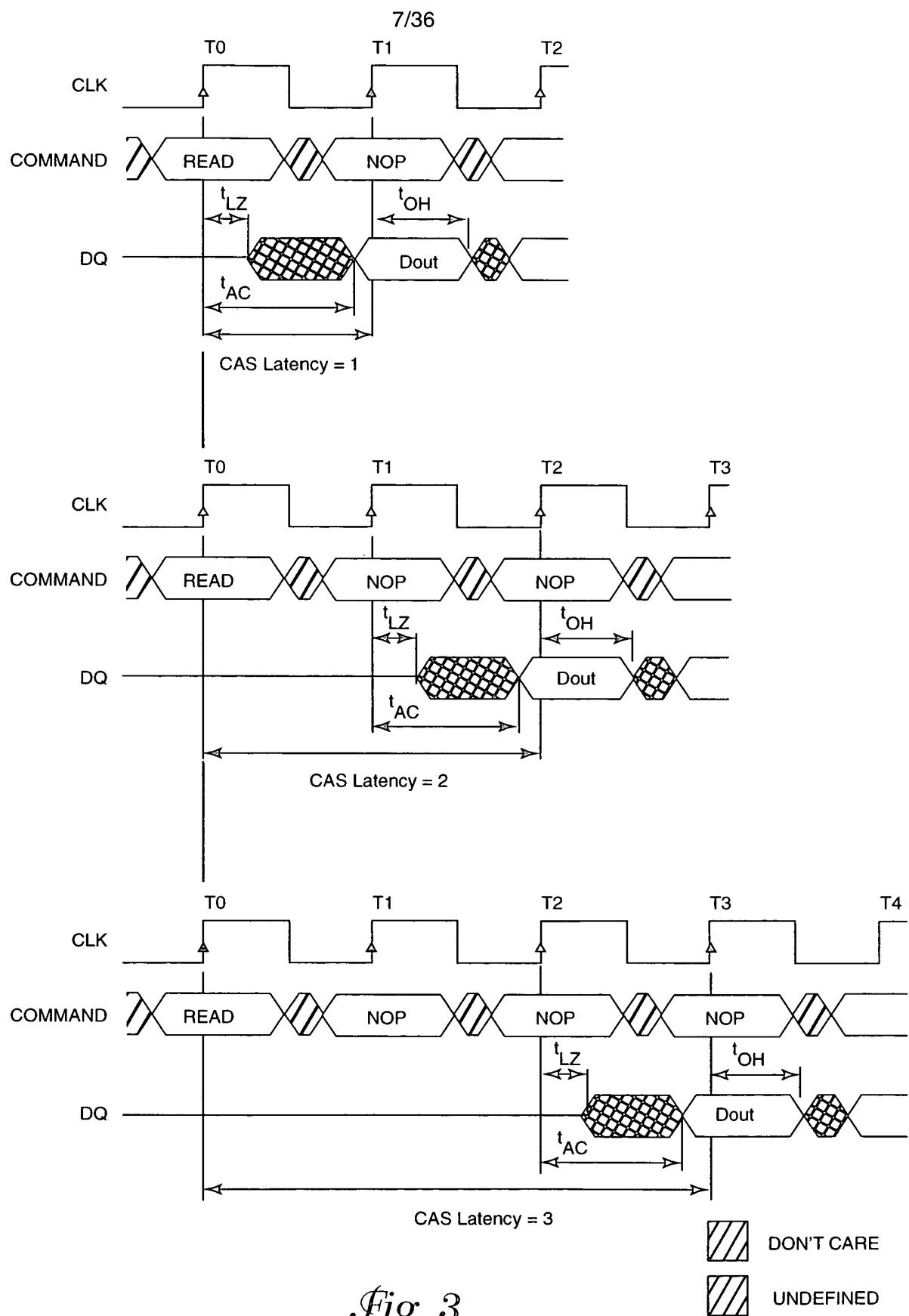


Fig. 3

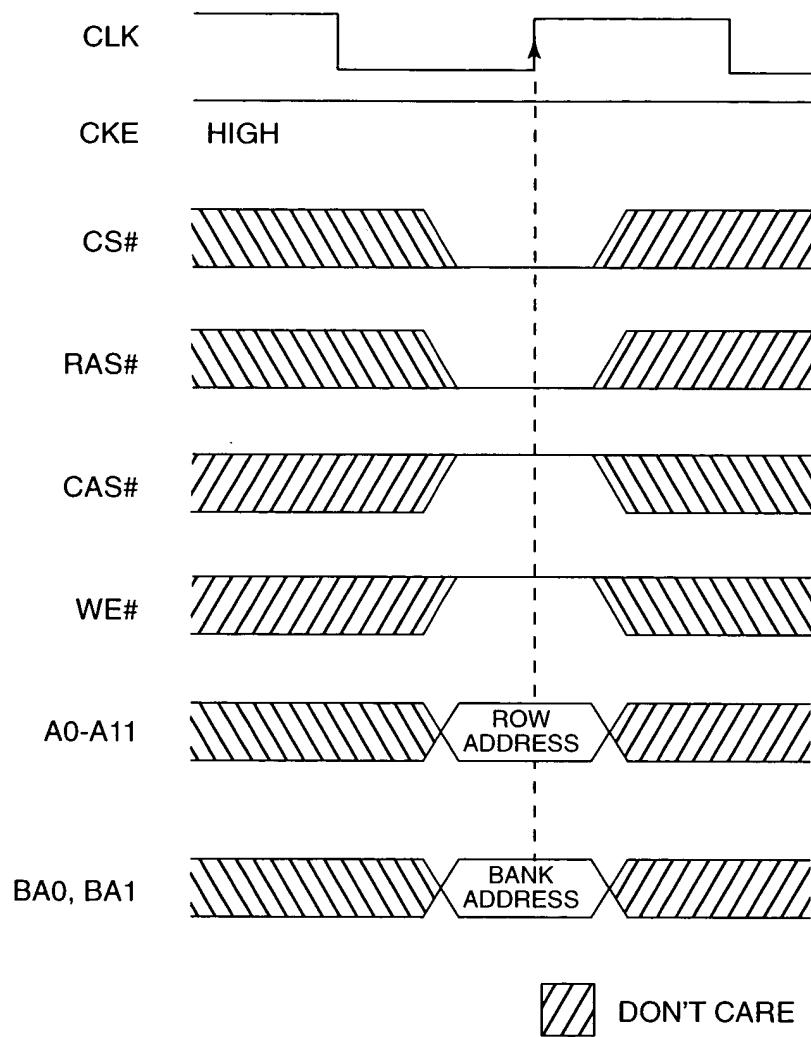
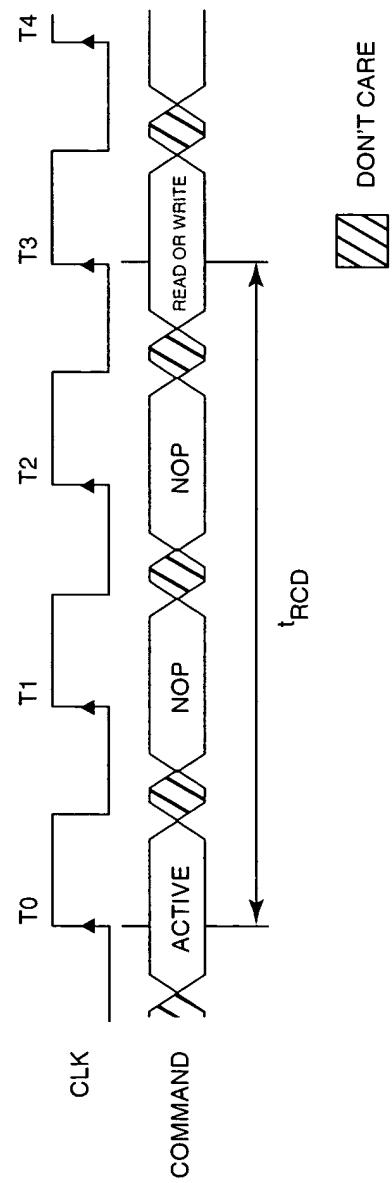
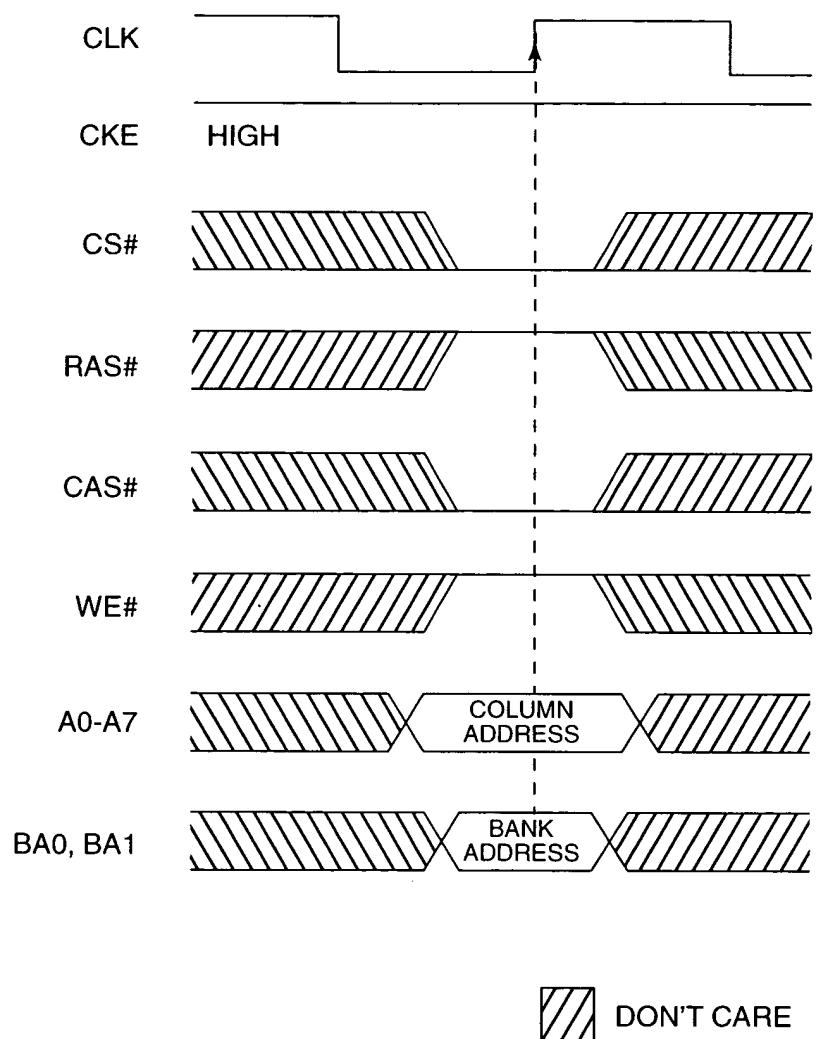
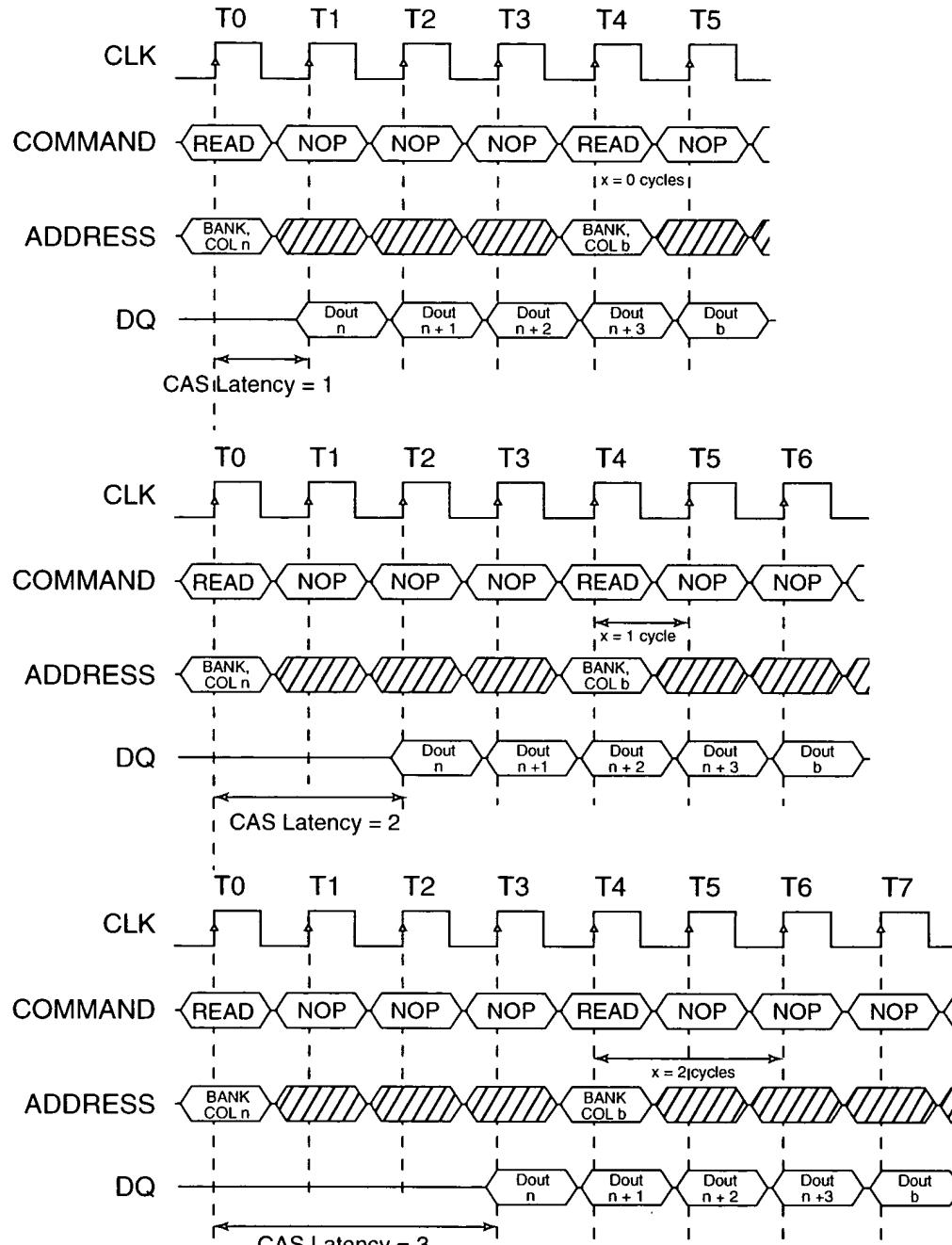


Fig. 4

*Fig. 5*

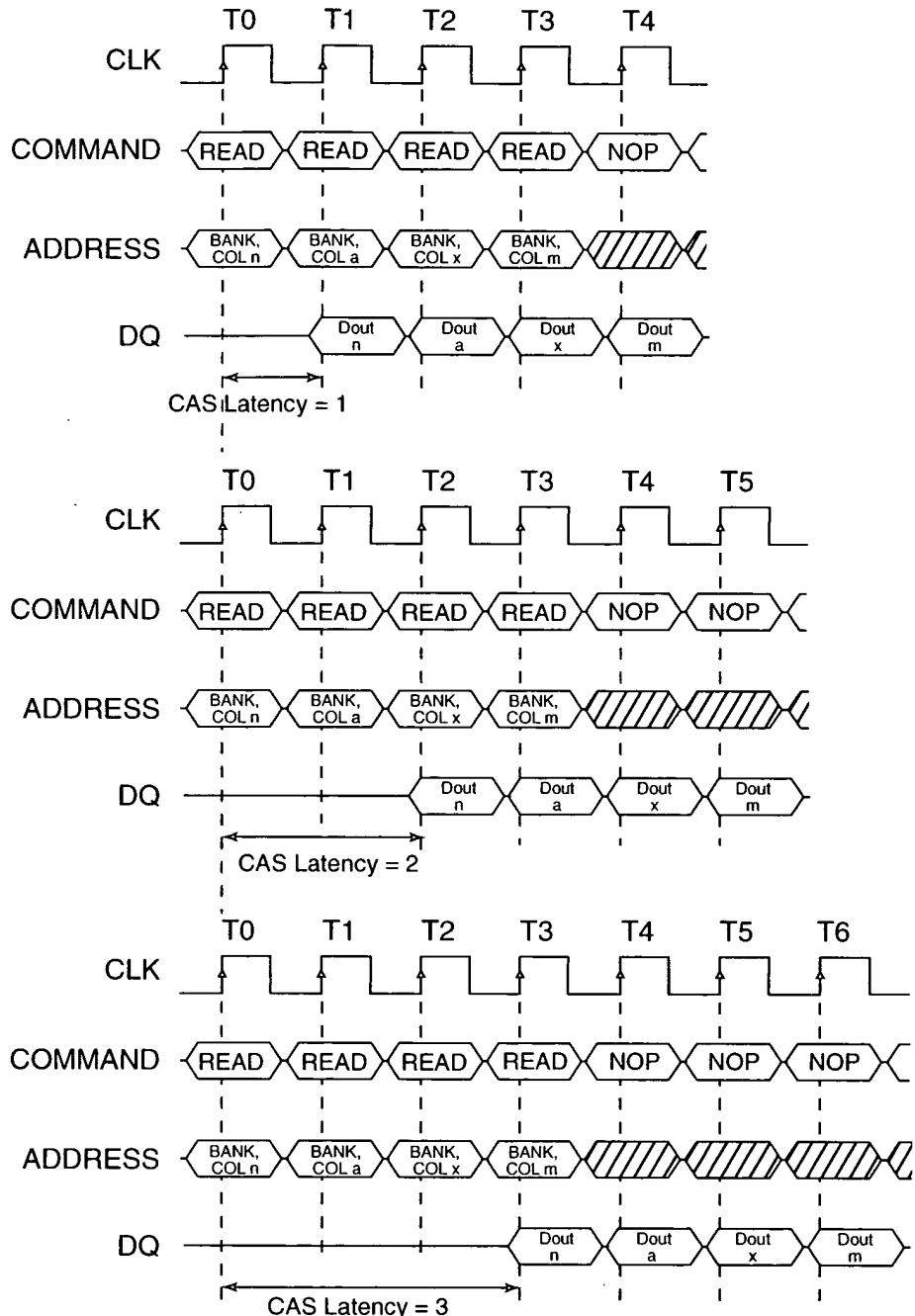
*Fig. 6*



DON'T CARE

NOTE: Each READ command may be to either bank. DQM is LOW.

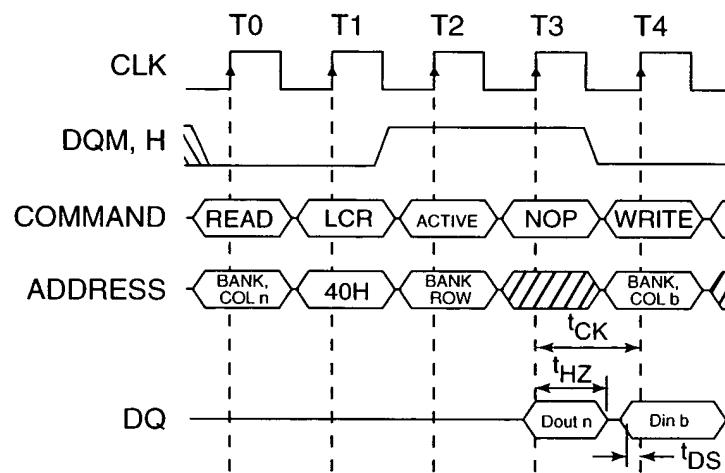
Fig. 7



DON'T CARE

NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 8



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DON'T CARE

Fig. 9

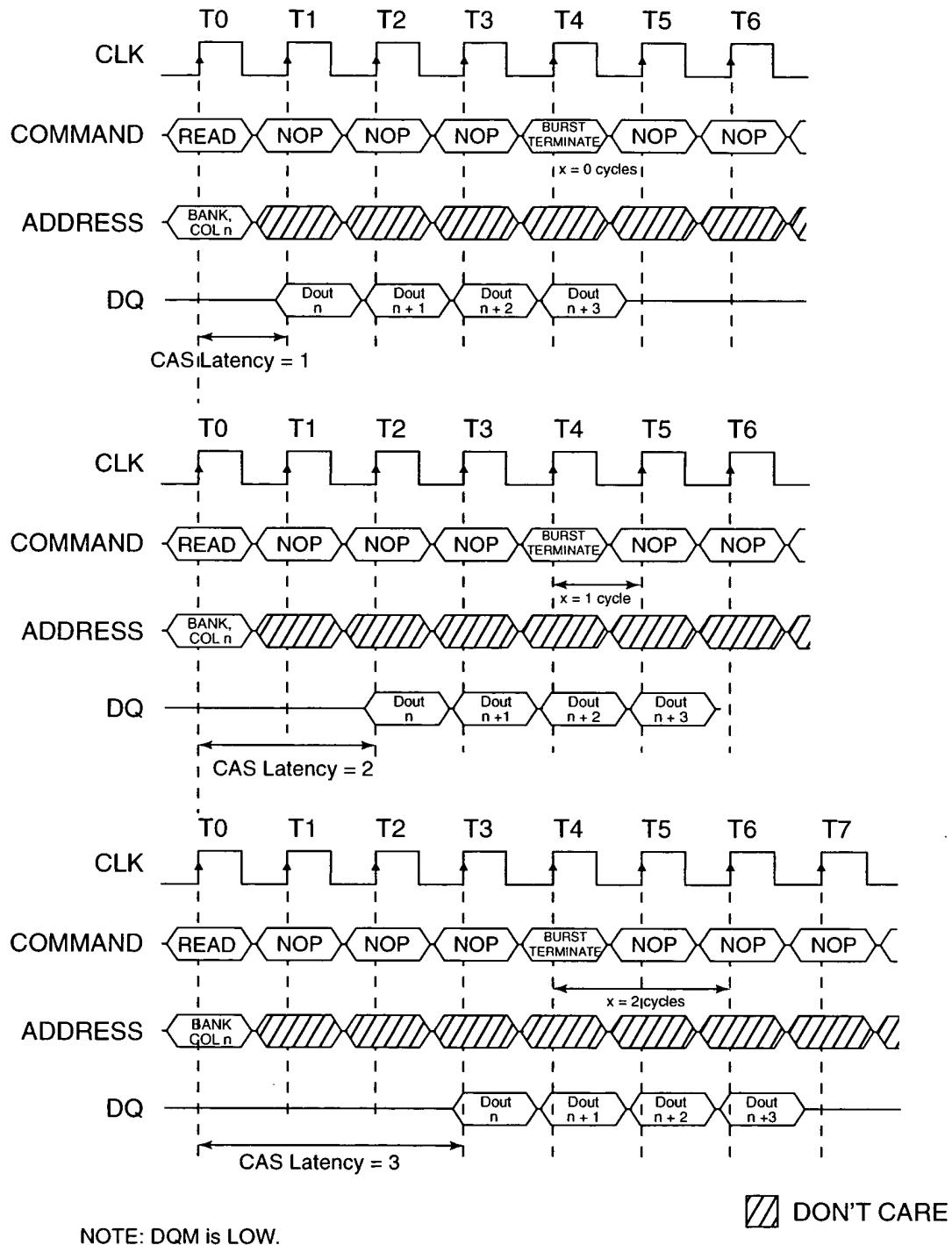
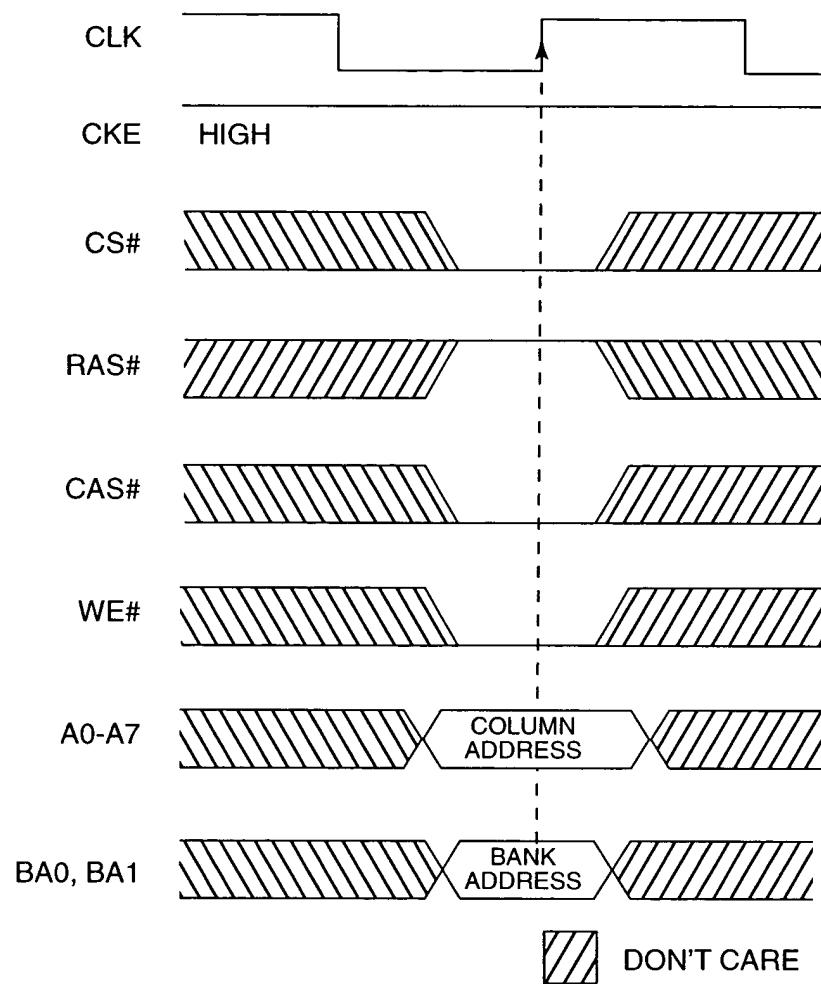
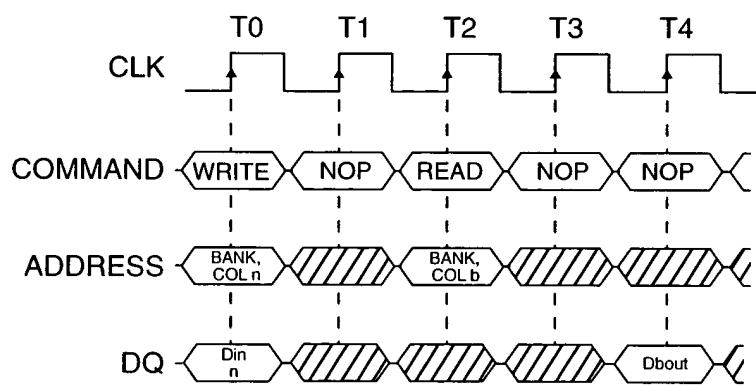


Fig. 10

*Fig. 11*



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data. For more details, refer to Truth Tables 4 and 5.

DON'T CARE

Fig. 12

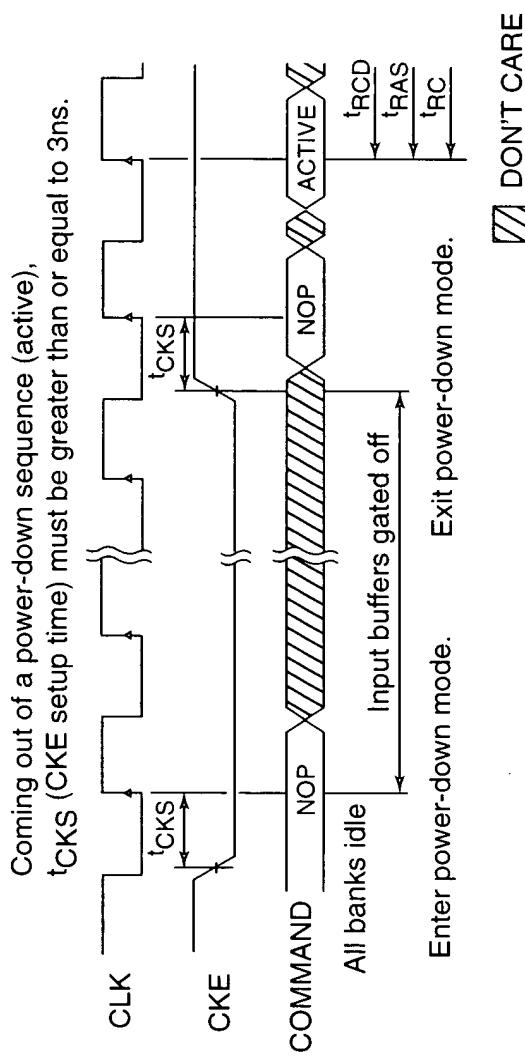
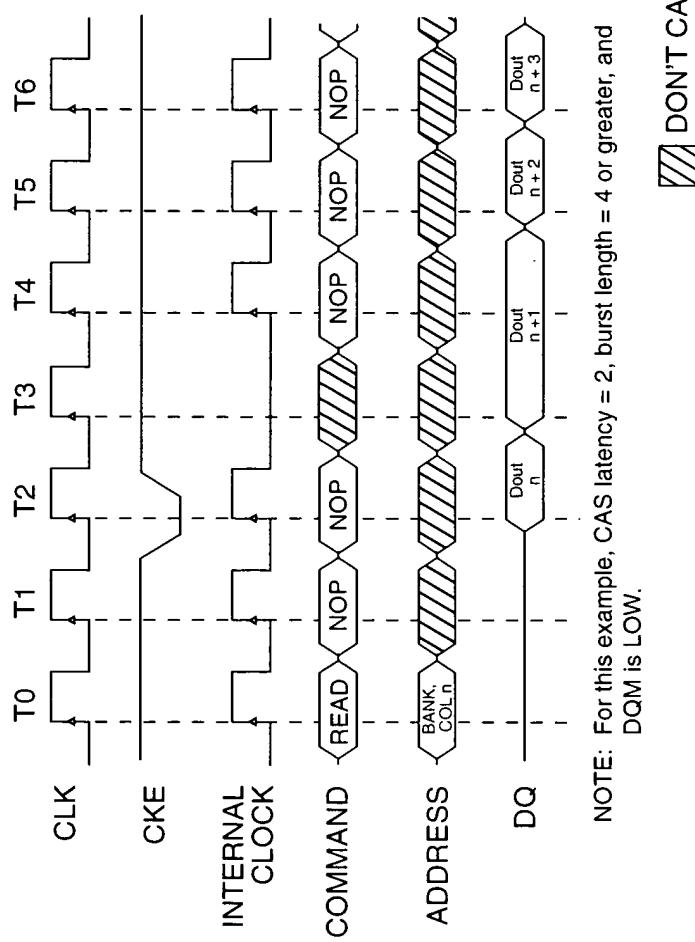
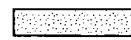


Fig. 13

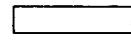
*Fig. 14*

ADDRESS RANGE			
	Bank	Row	Column
Bank 3	3	FFF FFH	256K-Word Block 15
	3	C00 00H	256K-Word Block 14
	BFF FFH	800 00H	256K-Word Block 13
	800 00H	7FF FFH	256K-Word Block 12
	7FF FFH	400 00H	256K-Word Block 11
	400 00H	3FF FFH	256K-Word Block 10
	3FF FFH	300 00H	256K-Word Block 9
	300 00H	2FF FFH	256K-Word Block 8
	2FF FFH	C00 00H	256K-Word Block 7
	C00 00H	BFF FFH	256K-Word Block 6
	BFF FFH	800 00H	256K-Word Block 5
	800 00H	7FF FFH	256K-Word Block 4
	7FF FFH	400 00H	256K-Word Block 3
	400 00H	3FF FFH	256K-Word Block 2
	3FF FFH	300 00H	256K-Word Block 1
	300 00H	2FF FFH	256K-Word Block 0
Word-wide (x16)			



Software Lock = Hardware-Lock Sectors

RP# = V_{HH} to unprotect if either the
block protect or device protect bit is set.



Software Lock = Hardware-Lock Sectors

RP# = V_{CCIO} unprotect but must be V_{HH}
if the device protect bit is set.

See BLOCK PROTECT/UNPROTECT SEQUENCE for
detailed information.

Fig. 15

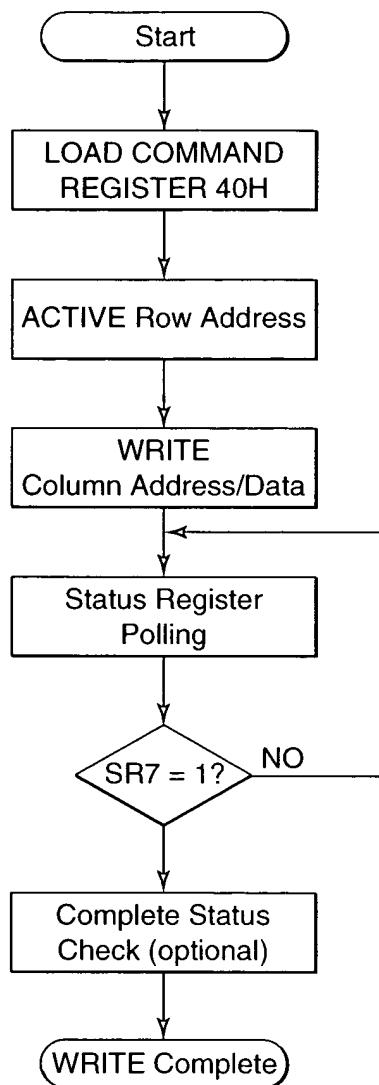


Fig. 16

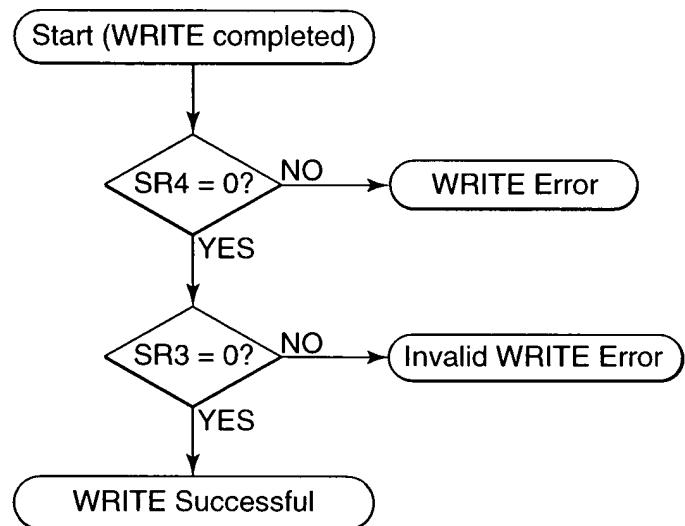


Fig. 17

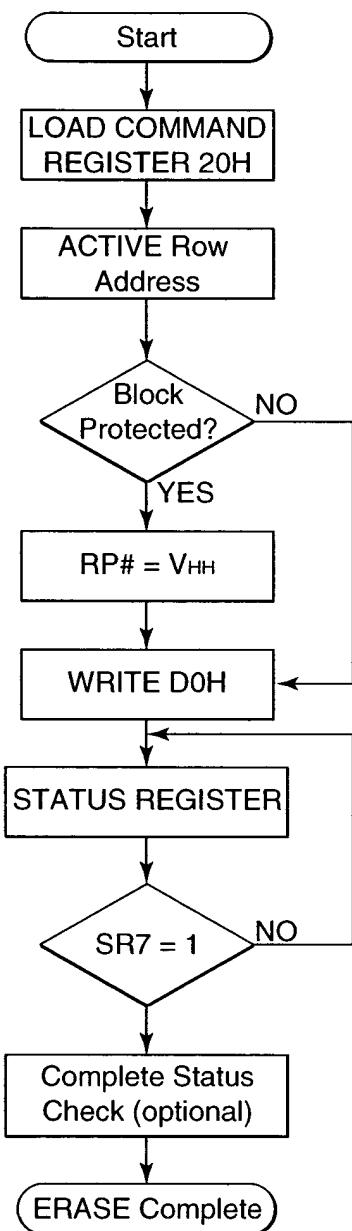


Fig. 18

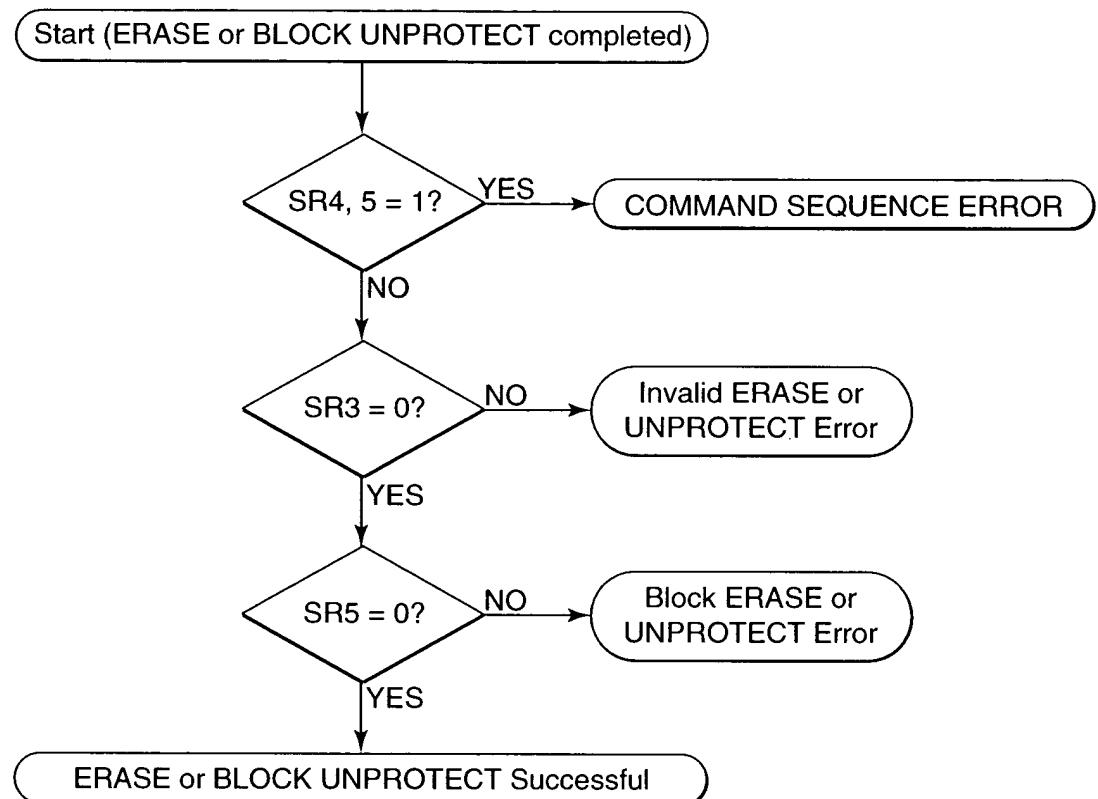


Fig. 19

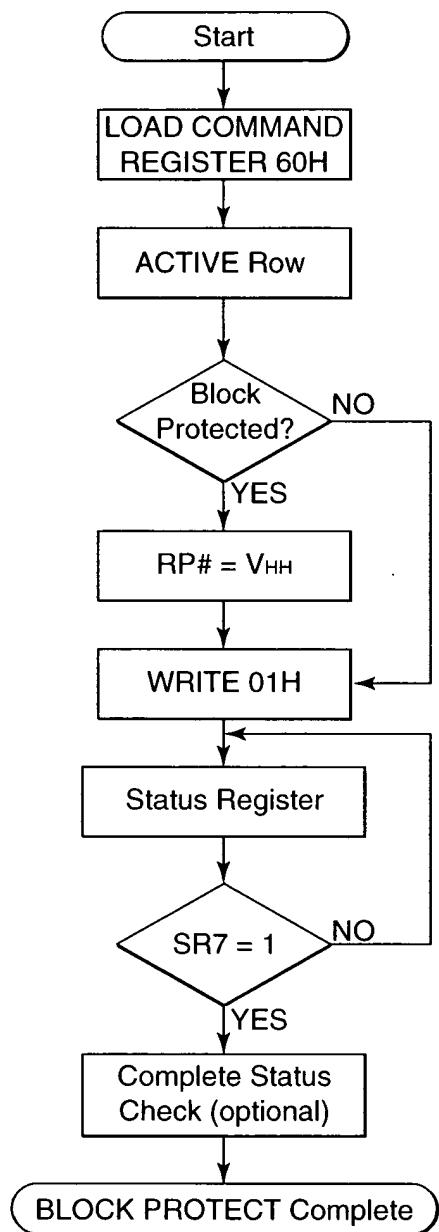


Fig. 20

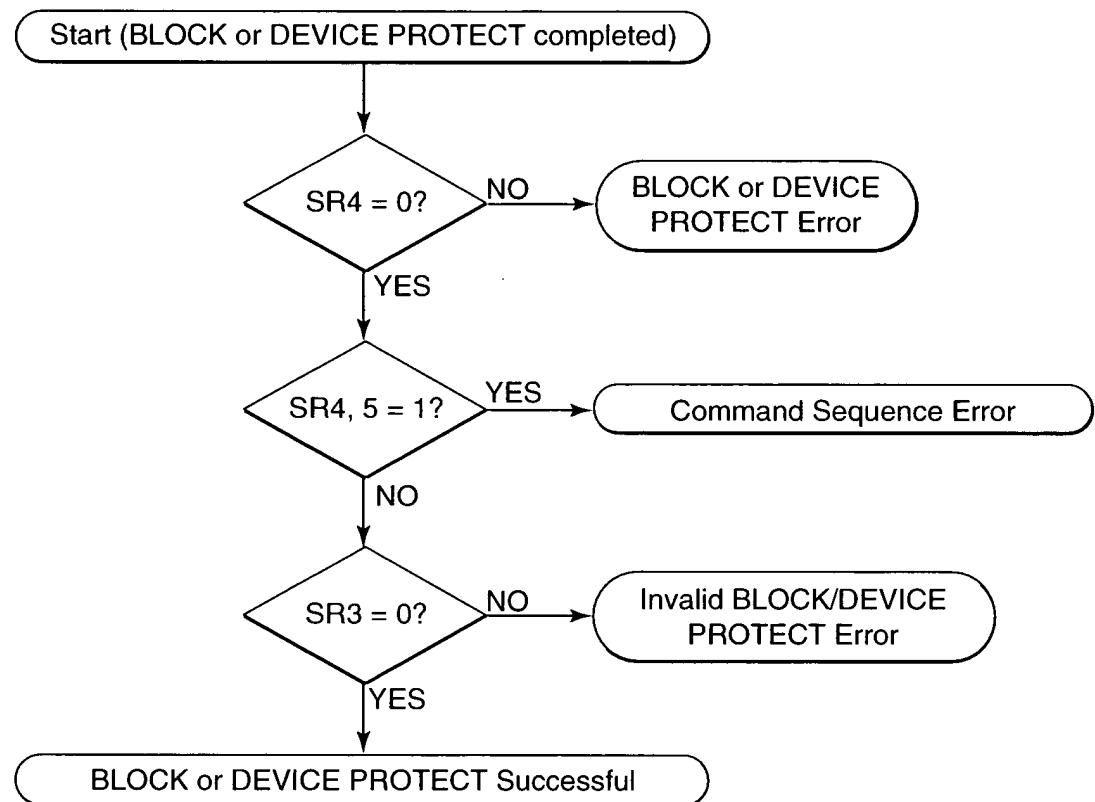


Fig. 21

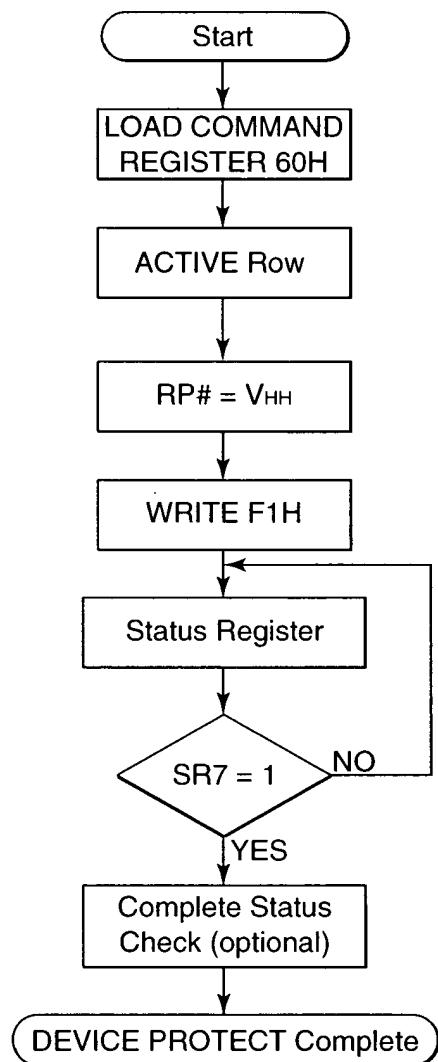
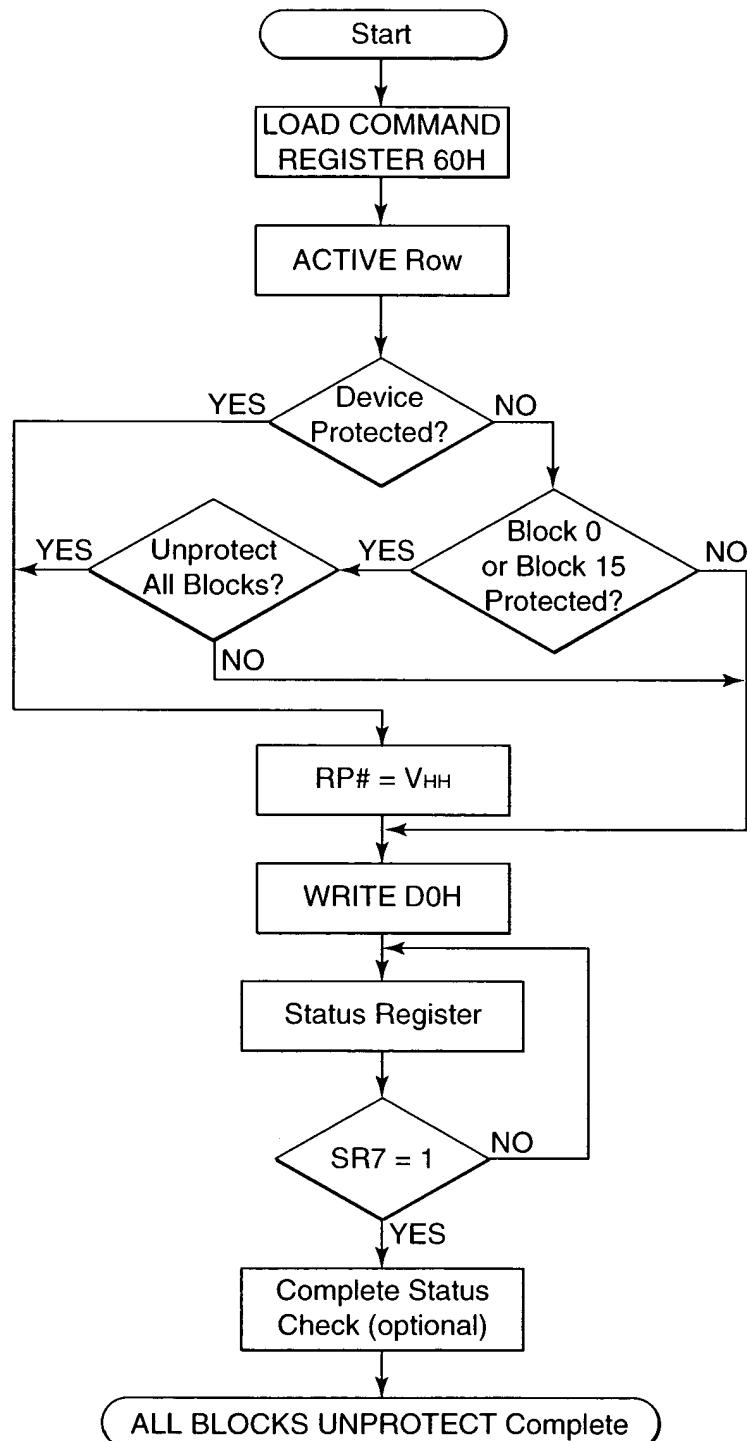


Fig. 22

*Fig. 23*

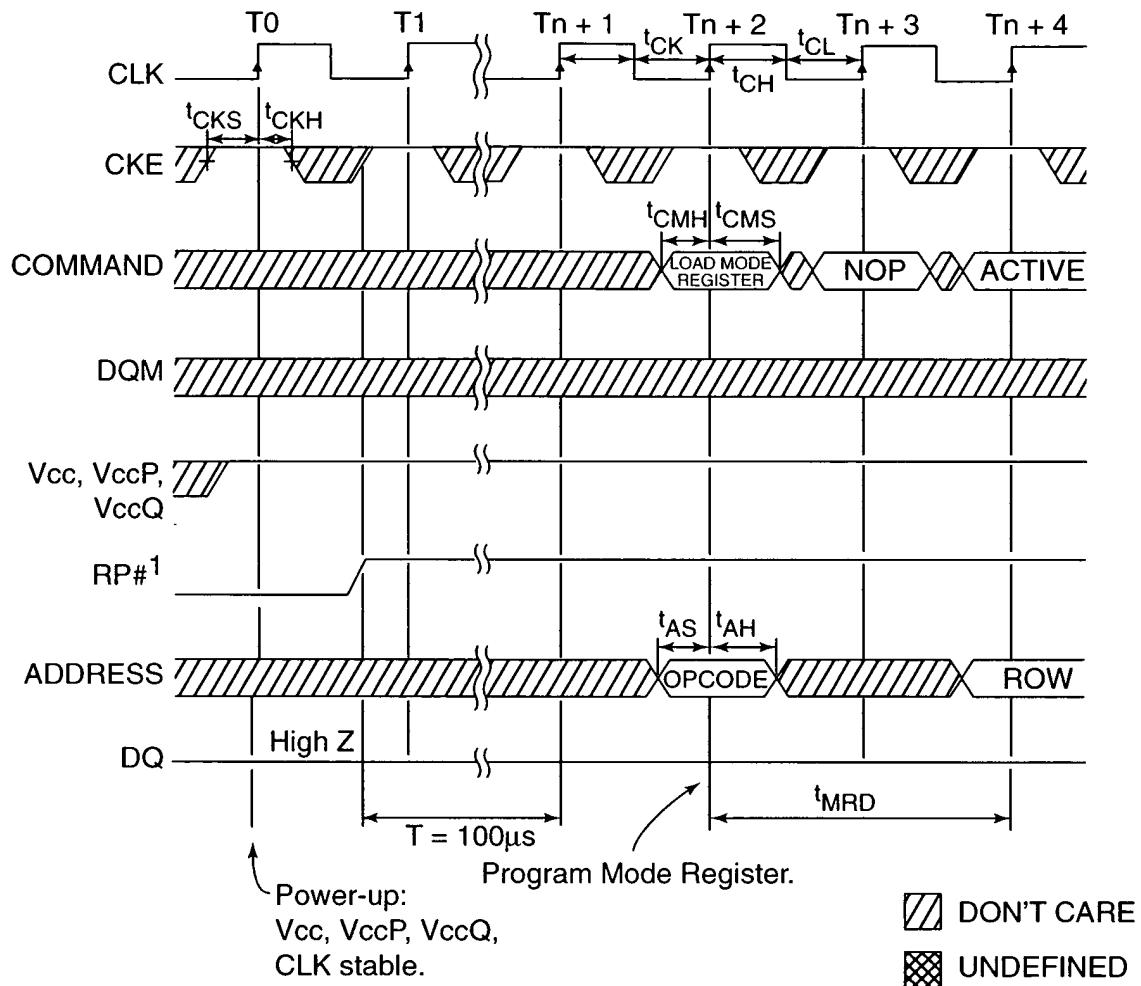


Fig. 24

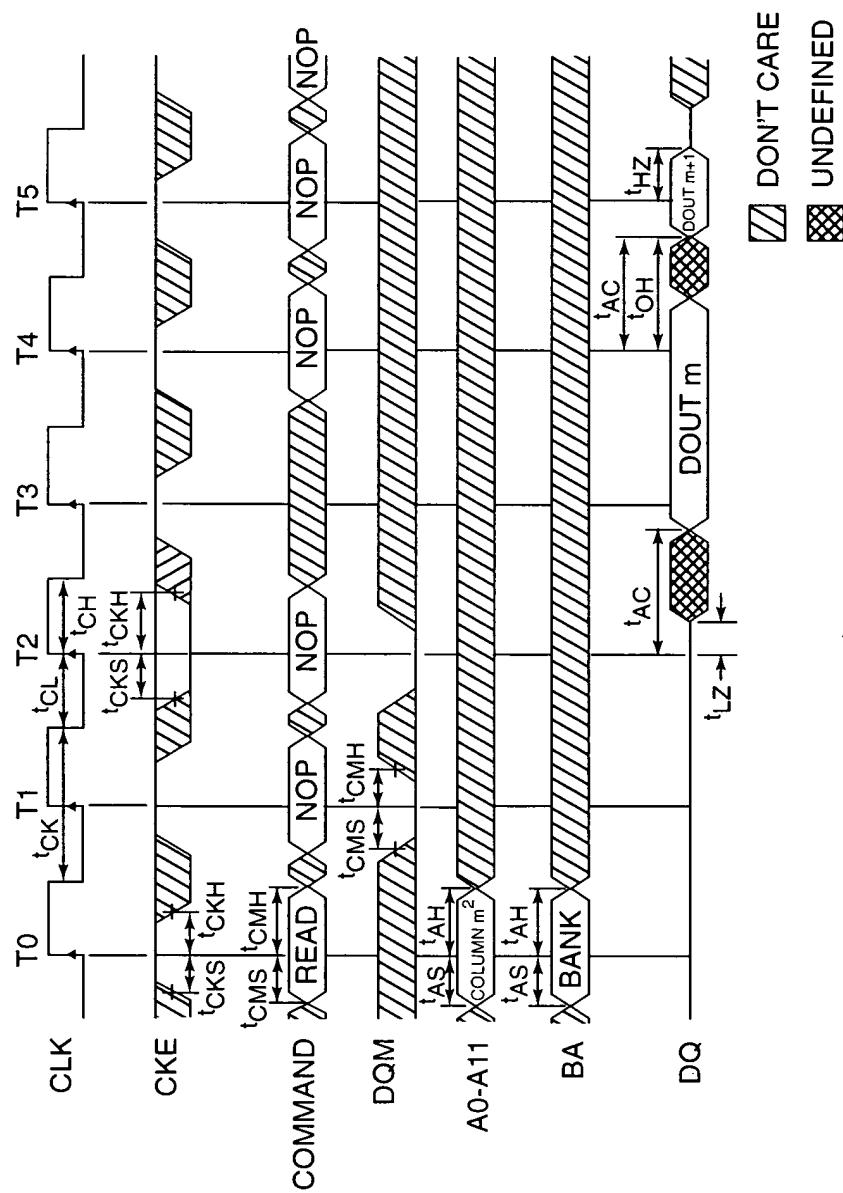


Fig. 25

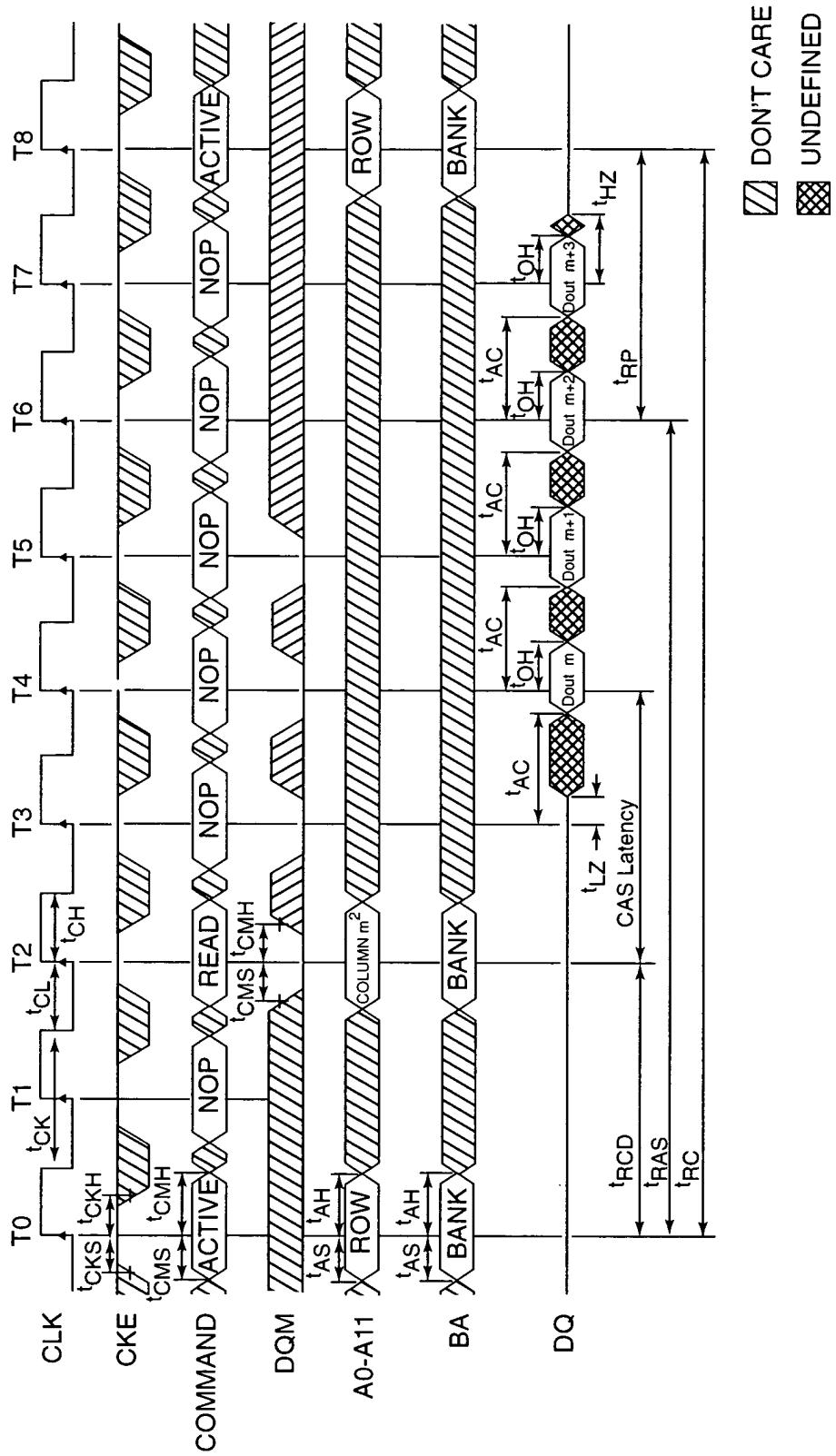


Fig: 26

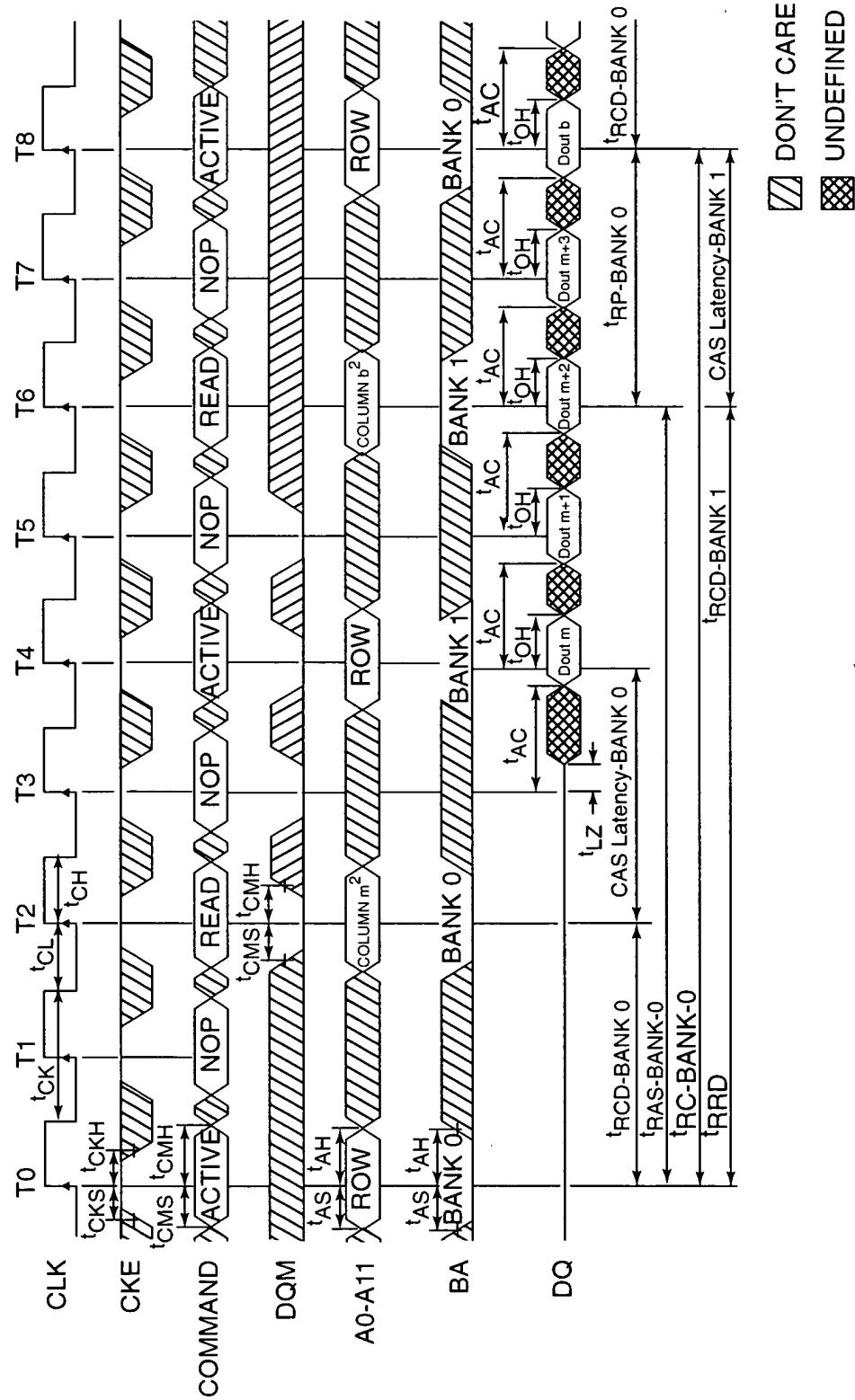


Fig. 27

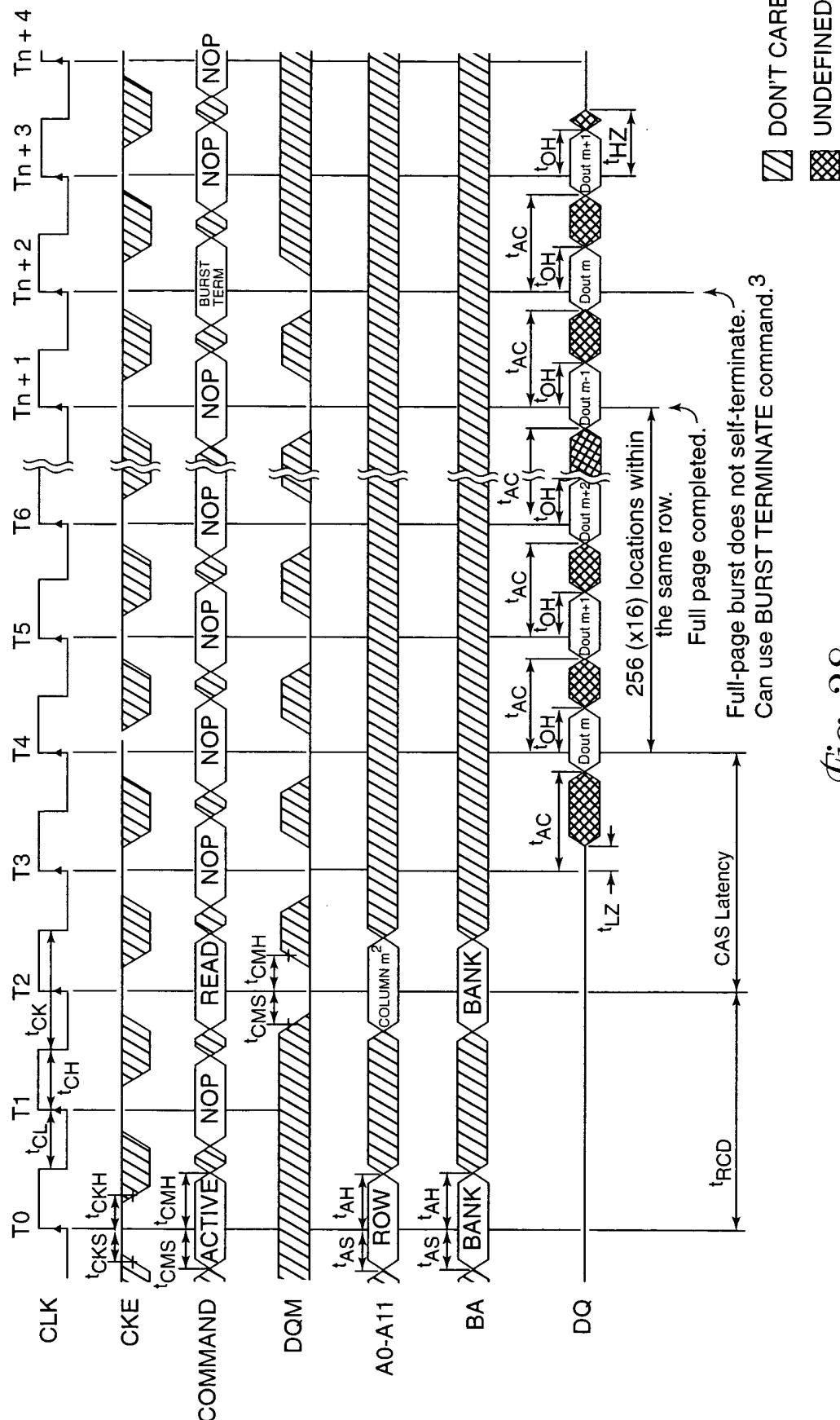


Fig: 28

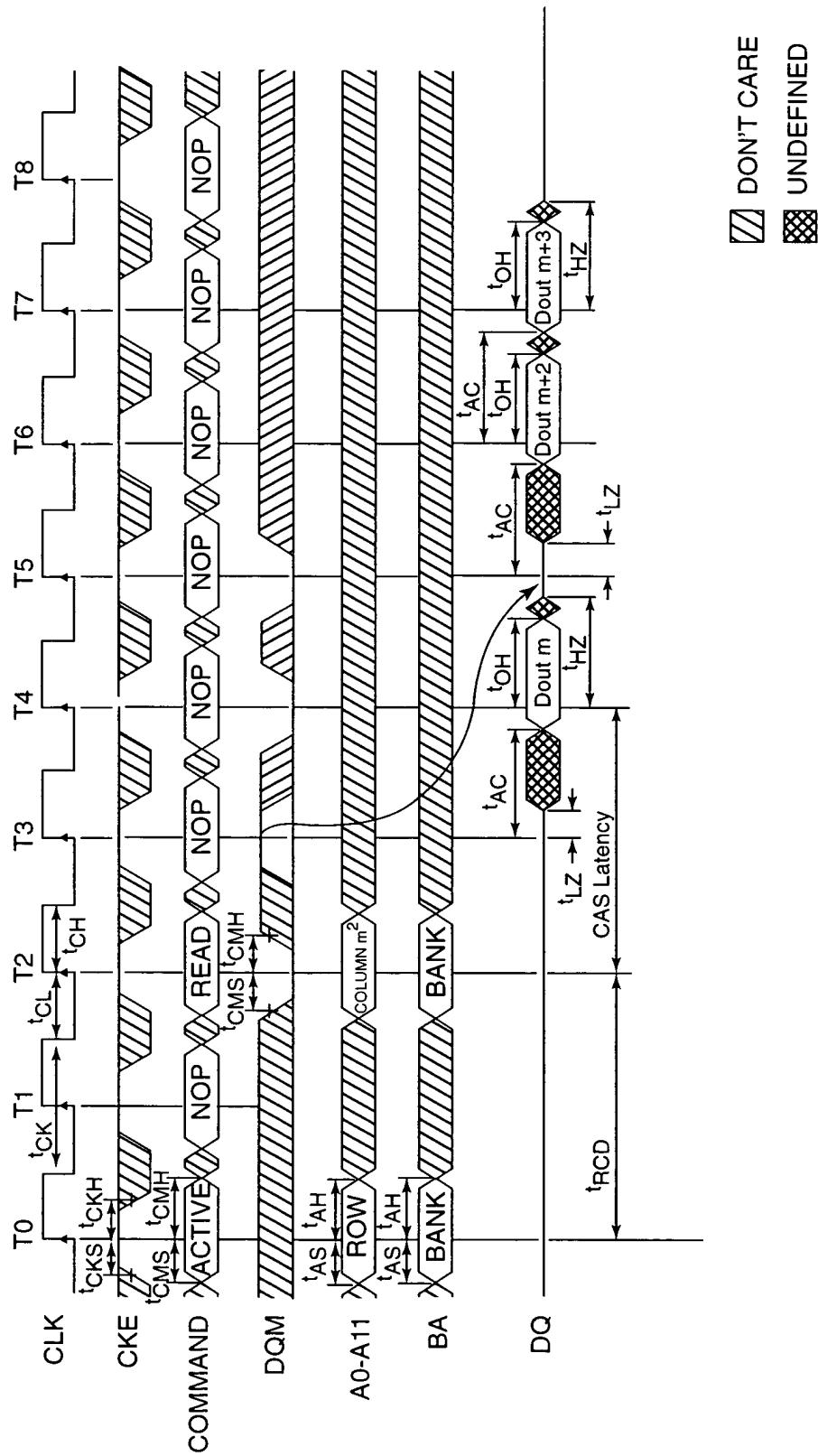


Fig. 29

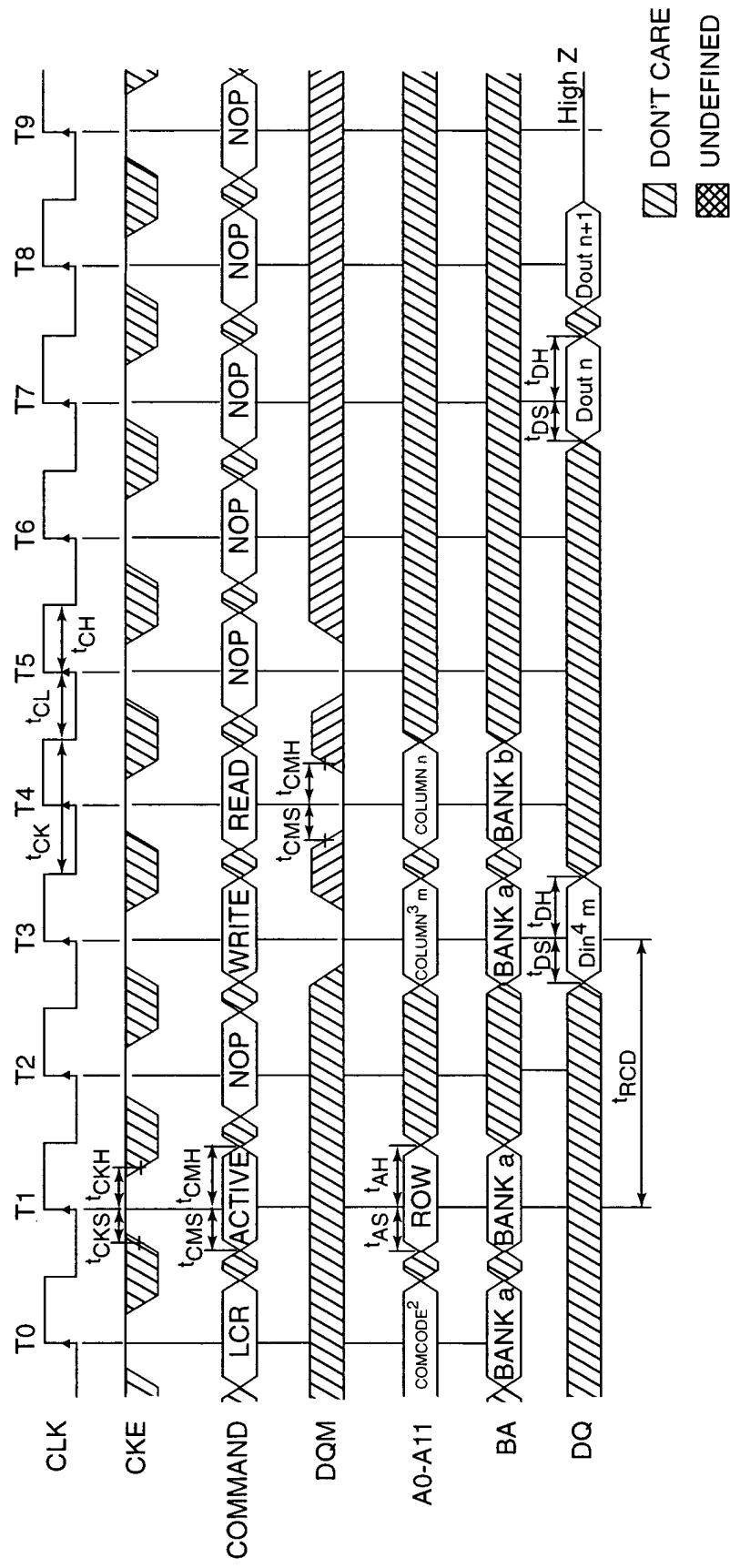


Fig. 30

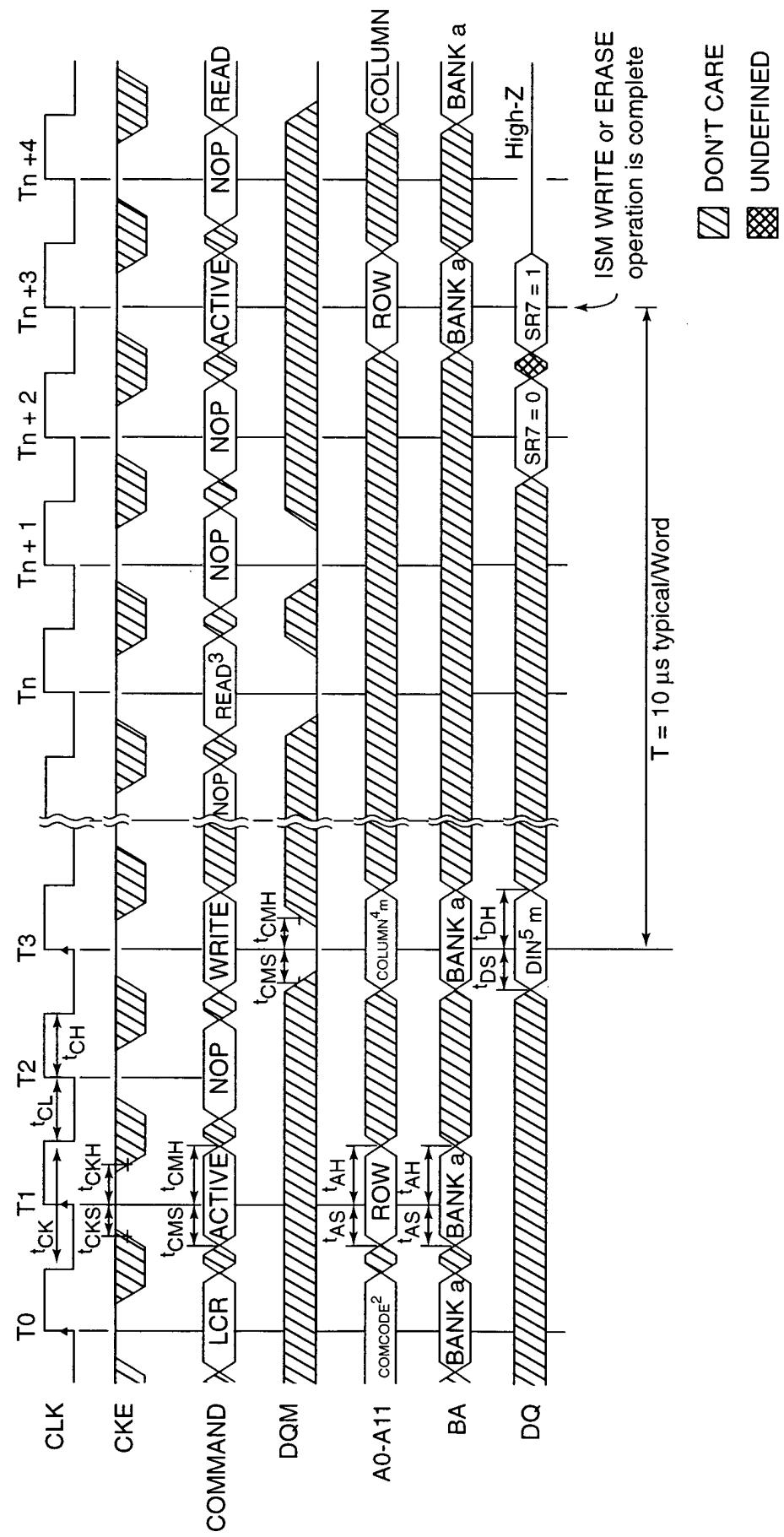


Fig. 31

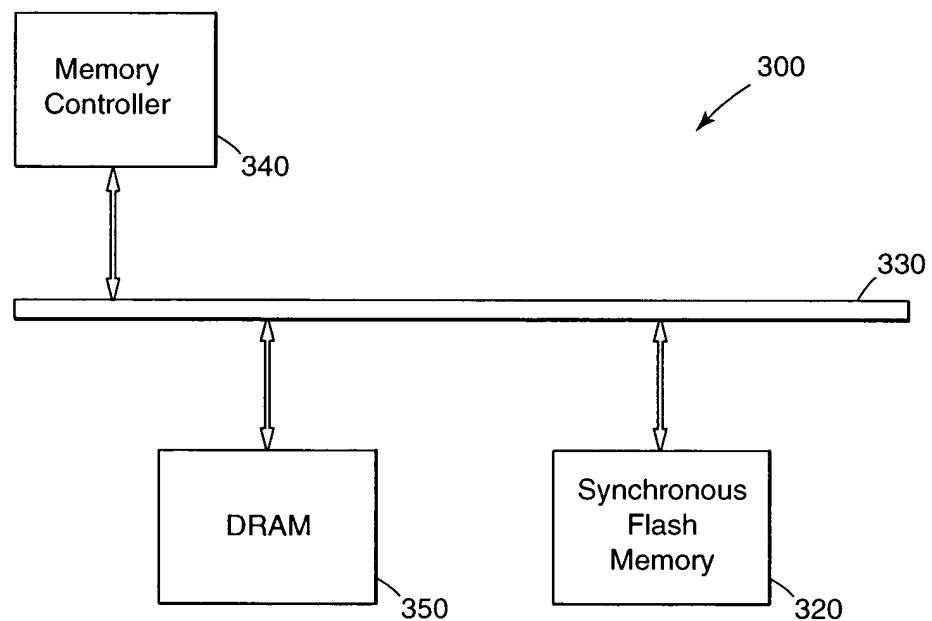


Fig. 32